A Modified Modulation Technique for Multilevel Converters with a Wide Range of Modulation Indexes and Minimized Harmonic Distortion at Low Indexes

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Abstract- *High switching losses, low switching speed and minimum turn-on and turn-off time are known as the main limitations of the semiconductor switches in high power converters. In applications such as variable speed drives, flexible ac transmission devices and active filters, a wide range of voltage variations are desirable. Therefore switching techniques applying in high power multilevel converters must consider above mentioned problems to have a good power quality and optimal efficiency for a wide range of modulation indexes.*

This paper presents a modified modulation technique with a wide range of modulation indexes and minimized harmonic distortion at low indexes. This method can be easily implemented for different converter topologies and for any number of levels. The minimum pulse restriction in diode-clamped converters and charge balance control for cascaded multilevel converters are considered in the proposed switching pattern. Simulation results of a three-phase seven-level cascaded converter validate the theoretical analysis with reasonable agreement.

Keywords: Multilevel Converter, Modulation index, Harmonic distortion reduction.

I. INTRODUCTION

Multilevel converters have been presented as a cost effective solution for various high voltage and high power applications including power quality and motor drive problems [1-7]. Many large variable speed drives, flexible ac transmission system devices and active filters may operate for long durations well bellow their rated capabilities, e.g. during the night period when production has stopped at a commercial or industrial facility. The multilevel inverters should be designed for the largest rated load. However, they also should be optimized to operate optimally over must of their operating region including at low amplitude modulation indexes. Therefore in these applications, with the requirement of the quality and efficiency and the limitation of high power device switching speed, low switching frequency, small THD and wide modulation index are desirable. By applying appropriate modulation schemes, these goals can be achieved simultaneously and therefore Modulation techniques play a very important role in multilevel converters.

Several modulation techniques have been developed and applied [8-11]. Stair case or stepped waveform modulation schemes eliminate lower frequency harmonics suitable for high power applications have been presented in [1-3] and [12]. These techniques require more than one switching per cycle to obtain a wide modulation index. The new stepped-waveform concept, which provides a wide range of modulation indexes is proposed in [13]. By using this technique, although with low switching frequency, wide modulation index can be achieved, but at very low indexes, THD of output waveforms increase strongly.

In this paper, the suggested technique can generate output stepped-waveforms with a wide range of modulation indexes and minimized distortion for the entire range of indexes. In general, the most significant low frequency harmonic components must be selected and eliminated. Then, high frequency harmonic components can be readily removed by using additional filters. Therefore the proposed modulation technique is to reduce DF (Distortion Factor) of line voltage. In motor drives, developed torque is proportional to current. Therefore in this case distortion of current is analyzed and compared to previous methods. Charge balance control for cascade multilevel converters and minimum turn-on and turn-off time for diode-clamped converters are considered in switching pattern, too. The computation effort is fairly simple to implement and is seamless for the entire range of modulation indexes. The simulation results of three-phase seven-level stepped-waveform converter show that a wide range of modulation indexes (from 0.05 to 1.05) as well as minimized harmonic distortion can be easily achieved by using the proposed technique.

II.MODIFIED MODULATION TECHNIQUE

A. Selective Harmonic Elimination, Conventional Method

Fig. 1 shows a quarter-wave symmetric stepped voltage waveform synthesized by a $2m+1$ level converter, where m is the number of switching angles. The waveform has no even

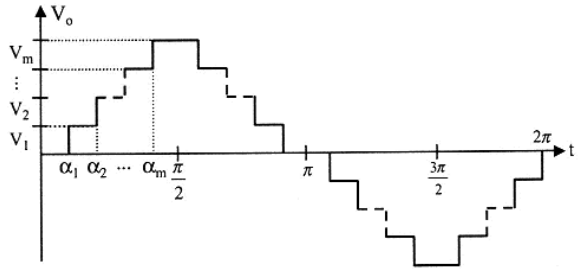


Fig. 1. 2m+1 level stepped voltage wave form.

harmonics. The amplitude of any odd harmonic of this stepped-waveform can be expressed as follows:

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) + \cos(n\alpha_2) + ... + \cos(n\alpha_m)] \quad (1)$$

Where V is the dc voltage, n is the odd harmonic order and α_K is the k-th switching angle.

According to Fig. 1, switching angles must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \alpha_3 < .....\alpha_m < \frac{\pi}{2} \quad (2)$$

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $m-1$ harmonic components can be removed from the voltage waveform. In general, the most significant low frequency harmonic components will be chosen to eliminate. Then, high frequency harmonic components can be readily removed by using additional filter circuits. Considering the Eq. (1), to have a constant number of eliminated harmonics, all switching angles ($\alpha_1,...,\alpha_m$) must be less than 90 degree. If the switching angles do not satisfy this condition, this scheme basically provides a limited range of modulation index [13]. For example, in a seven-level converter, its modulation index is only available from 0.5 to 1.05. The number of eliminated harmonic components decreases and distortion of voltage and current increases if the modulation index is lower than 0.5. As a result, it can be said that this technique provides a narrow modulation index range.

B. Wide Range Modulation

The polarity of some levels can be changed and as a result a low modulation index can be obtained [13]. As an example, consider a Three-phase seven-level stepped waveform. To minimize the DF of the line voltage and to achieve the adjustable amplitude of the fundamental component, the lowest significant non-triplen harmonic components must be eliminated from the synthesized phase voltage. In this case up to two surplus harmonics can be removed. Thus, the 5-th and 7-th harmonics, are chosen to be eliminated from the phase

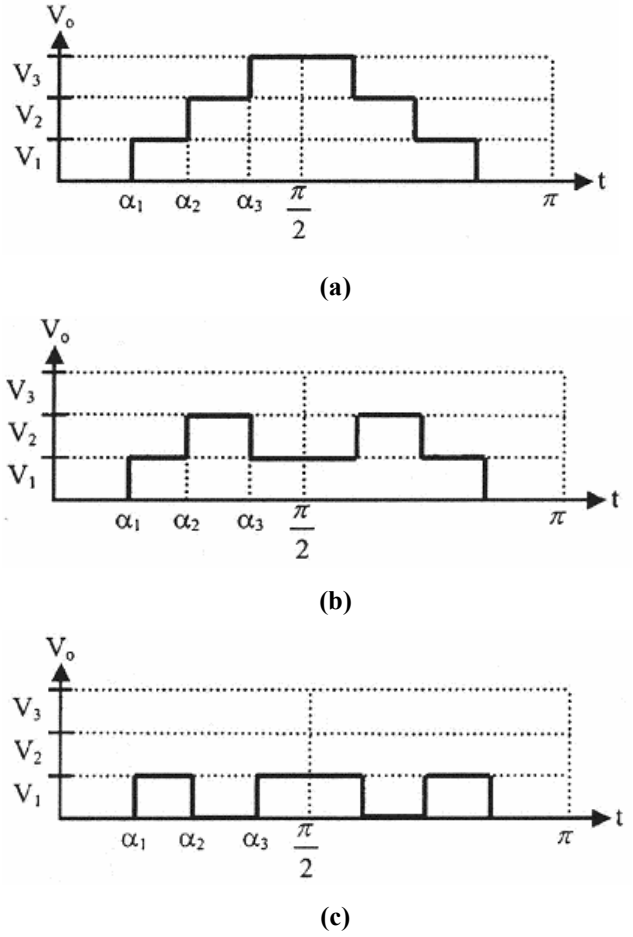


Fig. 2. A positive half cycle of a seven-level stepped-waveform with different modulation indexes. (a) High modulation index (b) Middle modulation index (c) Low modulation index.

voltages. Fig. 2 illustrates the positive half-cycle of seven-level stepped waveforms with different modulation index levels [13]. In this case the range of modulation indexes has been divided into three levels such as high, middle and low level. The amplitude of any odd harmonic of this stepped-waveform can be expressed by Eq. (3), whereas the amplitudes of all even harmonics are zero.

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] \quad (3)$$

Whenever α_3 is greater than 90, instead of this pattern, an output waveform shown in Fig. 2-b, which gives middle modulation index level, will be applied. Odd harmonics of this waveform in this level is expressed as follows:

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) + \cos(n\alpha_2) - \cos(n\alpha_3)] \quad (4)$$

An output waveform shown in Fig. 2-c will replace with Fig. 2-b if the switching angles α_1 to α_3 are not convergent at middle modulation index level. In this level the odd harmonics are:

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3)] \quad (5)$$

In general, a stepped-waveform, which comprises m switching angles, can be divided into m modulation index levels.

With the reduction of modulation index, fundamental component decreases but surplus harmonics are nearly constant. Therefore at low indexes, distortion of output waveforms increase strongly. As a result by using this technique, although with low switching frequency, wide modulation index can be achieved, but in very low indexes the distortion of output waveforms increase significantly.

C. Harmonic Reduction at Low Indexes

The modified technique of this paper can generate output voltage waveforms with a wide range of modulation indexes and minimized harmonic distortion in the entire range and at low indexes as well.

Fig. 3 shows a proposed quarter-wave symmetric stepped voltage waveform synthesized by a seven level converter at very low indexes. The amplitude of any odd harmonic of this stepped-waveform can be expressed by Eq. (6). In this case, allof even harmonics are zero too.

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) - \cos(n\alpha_4) + \cos(n\alpha_5) - \cos(n\alpha_6)] \quad (6)$$

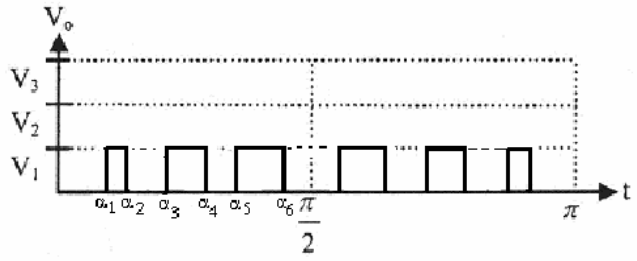


Fig. 3. Proposed switching pattern at very low modulation index

To minimize DF of line voltage, and to achieve adjustable amplitude of the fundamental component, up to five surplus harmonics can be removed. Thus, the 5-th, 7-th, 11-th, 13-th and 17-th harmonics, are chosen to be eliminated from the phase voltage. In this case the range of modulation indexes is divided into four levels such as high, middle, low and very low level. By using this technique, minimized harmonic in output waveforms and wide range of modulation indexes (from 0.05 to 1.05) can be achieved simultaneously. For the modulation index levels; high, middle and low, the main power devices switch only one time per cycle and in very low indexes switch two times per cycle, which is suitable for high power applications.

In general, a stepped-waveform, which comprises m switching angles can be divided into $m+1$ modulation index levels. Simulation results for seven-level converter, which is based on the suggested technique, will be presented in the section 4 of the paper.

III. Special Considerations

Fig. 1 shows a quarter-wave symmetric stepped voltage waveform synthesized by a $2m+1$ level converter.

Considering equations 3, 4 and 5 (and the Fig. 2 as well), the rising edge provides positive polarity for the corresponding cosine term, whereas the falling edge gives the cosine term a negative polarity. Equation 7 is the generalized form of the odd harmonic components in $2m+1$ level converter for all modulation indexes.

$$h_n = \frac{4V}{n\pi}[\cos(n\alpha_1) \pm \cos(n\alpha_2) \pm ..... \pm \cos(n\alpha_m)] \quad (7)$$

The positive and negative signs are for the rising and falling edges respectively. Only the polarity and the number of levels must be determined for different modulation indexes. Therefore the computation effort is seamless for the entire range of modulation indexes and is fairly simple to implement in various multilevel topologies.

A. Charge Balance Control

Cascade connected H-bridge multilevel converters are becoming an attractive topology for very high power applications. The dc link capacitor required in this converters are faced with a heavy stress. Limiting the DC bus voltage ripple to small magnitudes require large capacitors for all bridges. Thus, it is desirable to equalize bridge DC power over short period.

Pattern swapping scheme, shown in Fig. 4, make the cascade inverters voltage and current stresses the same and helps to maintain the batteries charge state balanced in high power hybrid electric vehicle (HEV) motor drives [10]. This scheme also can be used for equalizing the power drawn from each H-bridge of cascade converters in motor drives and FACTS devices, to reduce the size of the capacitor.

Switching pattern swapping scheme of the $2m+1$ level cascade converter, where m is the number of series connected H-bridges or the number of switching angles, is shown in table 1. For $2m+1$ level converter, this scheme needs at must m/2 cycles to equalize dc power drawn from all H- bridges.

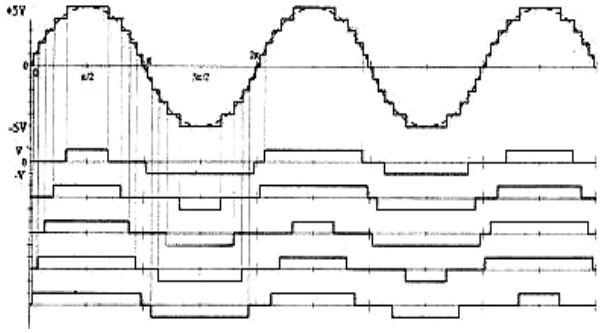


Fig. 4. Switching pattern swapping scheme of cascade inverter for balancing battery charge.

B. Minimum Pulse Limitation

Two well-known multilevel topologies are considered in term of how the minimum on-time and off-time (minimum pulse) affect their synthesized output waveforms[13].

Table 1. Switching pattern swapping scheme of the 2m+1 level cascade converter.

half cycle 1	half - cycle 2	.... ..	half - cycle m/2	half - cycle m/2+1
bridge 1	bridge m	....	bridge 2	bridge 1
bridge 2	bridge 1	....	bridge 3	bridge 2
::::::::::	::::::::::	::::	::::::::::	::::::::::
::::::::::	::::::::::	::::	::::::::::	::::::::::
bridge m-1	bridge m-2	....	bridge m	bridge m-1
bridge m	bridge m-1	....	bridge 1	bridge m

It is obvious that the minimum pulse is not required in cascade multilevel converters. Because narrow pulses can be produced by turning on the power switch from one bridge and turning off the power switch from another bridge. But for diode-clamped converters, the proper operation of high power semiconductor devices needs the consideration of the minimum pulse. If this restriction is not considered, high power semiconductor devices may fail and harmonic distortion increases. Therefore the greatest switching angle must take into account the minimum pulse. Because of symmetric characteristic of positive half cycle respect to 90° and negative half cycle respect to 270°, greatest switching angle (α_m) must satisfy the following condition, i.e.:

$$\alpha_m < 90 - \frac{pulse_{\min}}{2} \tag{8}$$

or,

$$pulse_{\min} = 360 ft_{\min} \tag{9}$$

or,

$$\alpha_m < 90 - 180 ft_{\min} \tag{10}$$

Where $t_{\min}$ is the duration of the minimum pulse (in second). To explain the approach numerically, assume that the minimum pulse for high power semiconductor switch is $150\mu\sec$. Considering Eq. (8) for a 50Hz system, $150\mu\sec$ is equal to 2.7°. From Eq. (10), α_m must be less than 88.65°. Therefore all switching angles must satisfy the following condition.

$$\alpha_1 < \alpha_2 < \alpha_3 < .....\alpha_m < 88.65^\circ \tag{11}$$

As a result, whenever α_m is greater than 88.65°, a switching pattern for different modulation index levels will be applied.

IV. SIMULATION RESULTS

Fig. 5 shows a three-phase seven-level cascade inverter which has been studied in this paper. Basically the modulation index for cascade multilevel waveform, M, is defined as follows.

$$M = \frac{h_1}{mV} \tag{12}$$

Where V is the dc voltage, h_1 is the amplitude of the fundamental component and m is the number of switching angles.

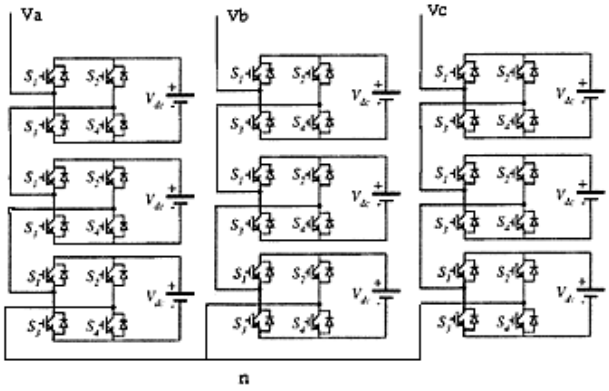


Fig. 5. Three phase seven-level cascade inverter

Distortion factor (DF) of line voltage is defined as follows:

$$DF(\%) = \frac{\sqrt{\sum_{n=2}^{200} [\frac{h_n}{n^2}]^2}}{h_1}.100 \quad (13)$$

Where h_n is the amplitude of n-th harmonic.

In motor drives, torque is proportional to current. Therefore in this case distortion of current is analyzed. Total line current harmonic distortion is definedas follows:

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{200} (\frac{h_n}{n})^2}}{h_1}.100 \quad (14)$$

To minimize harmonic distortion, 5-th and 7-th harmonics must be eliminated from the phase voltage. Thus, a set of nonlinear equations, in high modulation level, are derived as follows:

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = \frac{3m\pi}{4} \quad (15)$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) = 0 \quad (16)$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \quad (17)$$

To solve this nonlinear equations the Newton-Raphson method has been used [9,14]. Equations which should be solved for all modulation indexes are given in appendix. Angles calculated for each index are initial values for solving these nonlinear equations for the next index. Fig. 6-a shows calculated switching angles (α_1, α_2 and α_3) versus high modulation indexes. As it can be seen, with the reduction of the modulation index, α_3 increases and at index 0.49, α_3 is equal to 88.1°. According to Eq. (10), all switching angles must be less than 88.65°. Whenever α_3 is greater than 88.65°, this waveform is no longer exist. Therefore, an output waveform shown in Fig. 2-b, which is proper for middle modulation index level, will be applied instead.

When the switching angles α_1 to α_3 in Fig. 2-b are not convergent at middle modulation index level, an output waveform shown in Fig. 2-c will replace.

Fig. 6-b and 6-c illustrate switching angles, α_1, α_2 and α_3, versus middle and low modulation indexes, respectively. Fig. 3 shows the switching pattern at very low modulation indexes. As shown in Fig. 7 all switching angles in this level are smaller than 88.65°. Waveforms and spectra of line voltage are shown in figures 8 and 9. As expected, the results show that 5-th, 7-th, 11-th, 13-th and 17-th harmonic components of the line voltage at very low modulation indexes and all triplen harmonics in line voltages are very small.

Although all switching angles in all levels satisfy the condition of Eq. (10) and the range of modulation indexes is wide, but at very low indexes DF and THD increase strongly. Figures 10 and 11 present the DF and THD of the proposed technique and the technique which is suggested earlier [13]. As it can be seen, the proposed technique of the paper reduces the DF of line voltage up to 80% and THD of line current up to 58% of the other technique.

V. CONCLUSIONS

A modified modulation technique for multilevel voltage source converters, suitable for large variable speed drives, high voltage power supplies and flexible ac transmission system devices has been presented in this paper. The proposed technique can generate stepped waveforms with a wide range of modulation indexes (from 0.05 to 1.05), as well as minimized harmonic distortion. This method is simple to implement in varies multilevel converter topologies and for any number of levels. The computation effort is seamless for the entire range of modulation indexes.

A three-phase seven-level cascaded inverter is simulated as an example. The simulation results validate the theoretical analysis with reasonable agreement.

REFERENCES

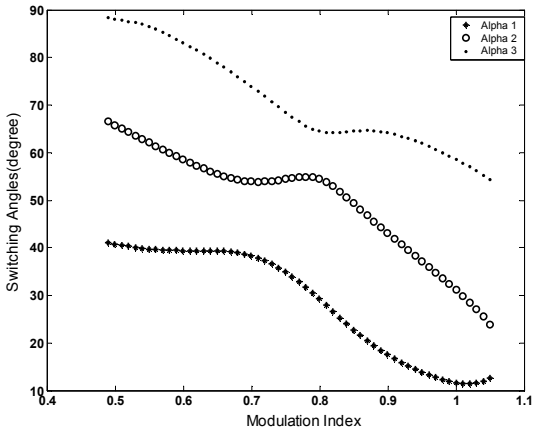
[1] L. M. Tolbert, F. Z. Peng and T. J. Habetler, "Multilevel converters for large electric drives", IEEE Trans. on Industry Applications, Vol. 35, No. 1, pp. 36-44, Jan/Feb 1999.

[2] F. Z. Peng, J. W. McKeever and D. J. Adams," A power line conditioner using cascade multilevel inverters for distribution systems", IEEE Trans. on Industry Applications, Vol. 34, No. 6, pp. 1293-1298, Nov/Dec 1998.

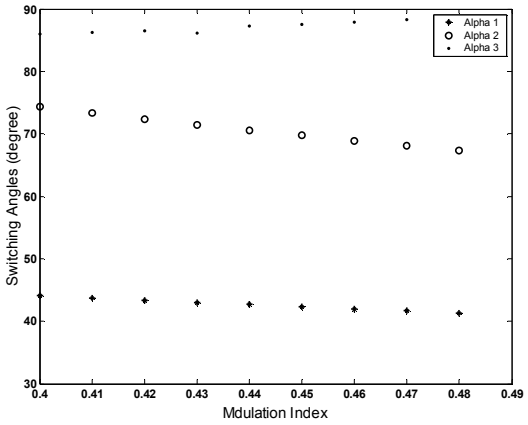
[3] F. Z. Peng and J. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters", IEEE Trans. on Industry Applications, Vol. 33, No. 3, pp. 748-755, May/June 1997.

[4] M. Calais, L. J. Borle and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single phase five-level inverter ", IEEE Power Electronics Specialists Conf. pp. 1351-1356, 2001.

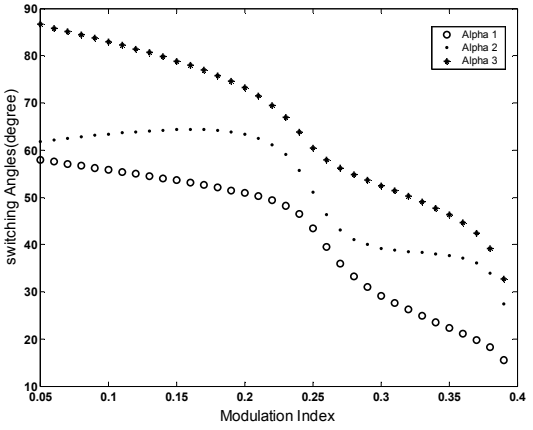
[5] D. A. Rendusara, E. Cengelsi, P. N. Enjeti, V. R. Stefanovic and J. W. Gray, "Analysis of common mode voltage –"neutral shift" in medium voltage PWM adjustable speed drive (MV-ASD) systems", IEEE Trans. on Power Electronics, Vol. 15. No. 6, pp. 1124-1133, November 2000.



(a)



(b)



(c)

Fig. 6. Switching angles versus modulation indexes. (a) High, (b) Middle and (c) Low modulation indexes.

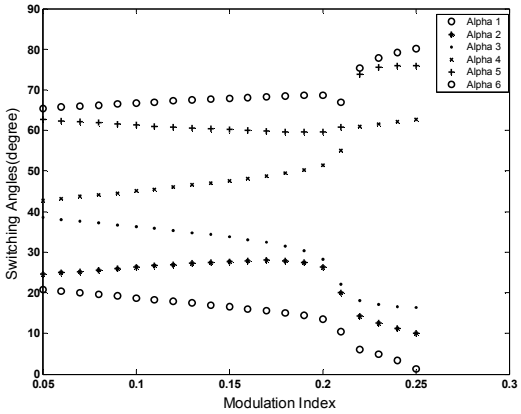


Fig. 7. Switching angles versus modulation indexes in very low modulation indexes.

[6] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems", IEEE Power Engineering Society Summer Meating, pp. 1271-1274, 2000.

[7] J. Rodriguez, L. Moran, A. Gonzalez and C. Silva, "High voltage multilevel converter with regeneration capability ", IEEE Power Electronics Specialists Conf, pp. 1077-1082, 1999.

[8] J.Pitel,S.N.Talukdar ,P. Wood, "characterization of Programmed –Waveform Pulsewidth Modulation ," IEEE Trans. on Ind. Appl ., Vol.IA-16,No5 , Sep ,1980 , pp.707-715.

[9] G. Carrara, S.Gardella,M.Marchesoni, R. Salutari, G. Sciutto, " A New Multilevel PWM Method : A Theoretical Analysis," , Proc. of IEEE Power Electron. June , 1990 , pp.363-371.

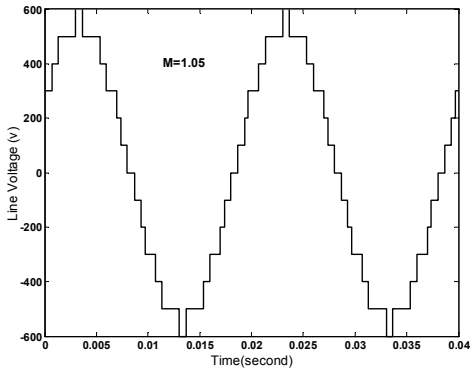
[10] S. R. Bows, "New sinusoidal pulse with-modulated inverter," Proc. IEE , Vol.122, No.11, Nov. 1975.

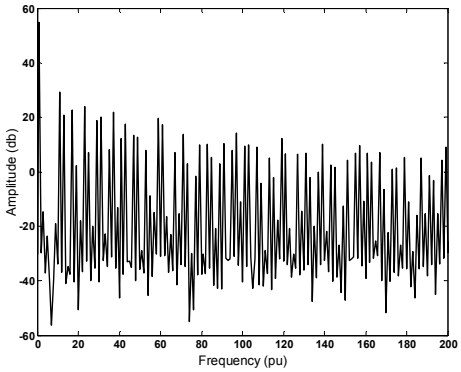
[11] H. S. Patel, R. G. Hoft, "Generalized of harmonic elimination and voltage control in Thyristor inverter: part I-harmonic elimination", IEEE Trans. on Ind. Appl., Vol.IA.9, NO.3, May/Jun., 1973, pp.310-317.

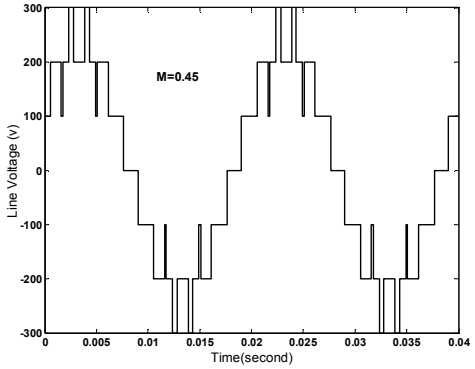
[12] R. Kiefernorf, G.Venkataramanan and M. D. Manjrakar, "A power electronic transformer (PET) fed nine-level H-bridge inverter for large induction motor drives ", IEEE Industry Applications Conf, pp.2489-2495,2000.

[13] S. Sirisukprasert, L. Jih-Sheng and L. Tian-Hua, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters",IEEE Trans. on Industrial Electronics, Vol.49, No.4, August 2002.

[14] J. Sun, H. Grotstollen, "Solving nonlinear equations for selective harmonic eliminated PWM using predicted Initial values", in Proc. IECON 1992, pp.259-264.







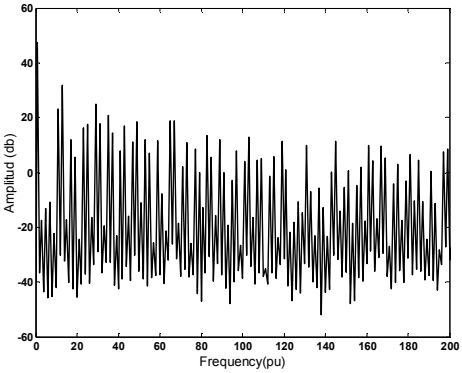
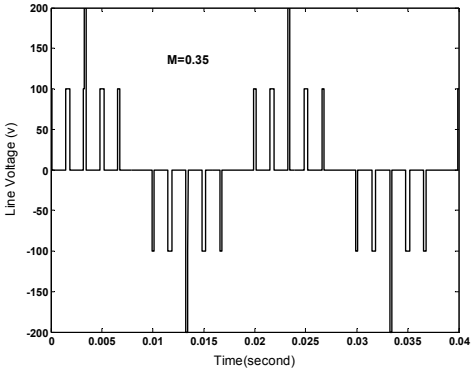
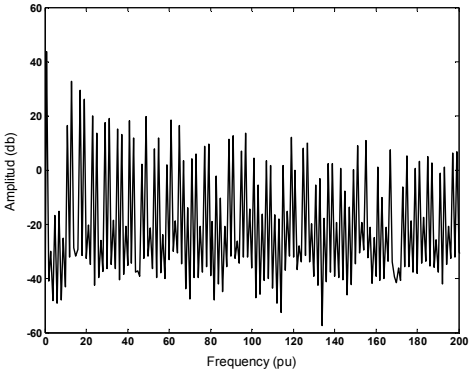
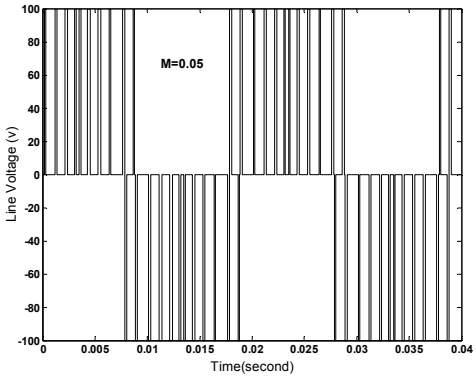


Fig. 8.
Line voltage waveform and spectra in high and middle modulation index levels, respectively







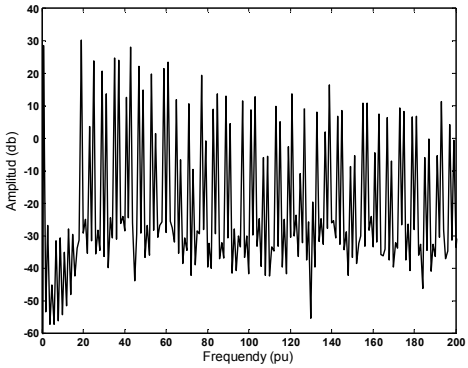


Fig. 9.
Line voltage waveform and spectra in low and very low modulation index levels, respectively

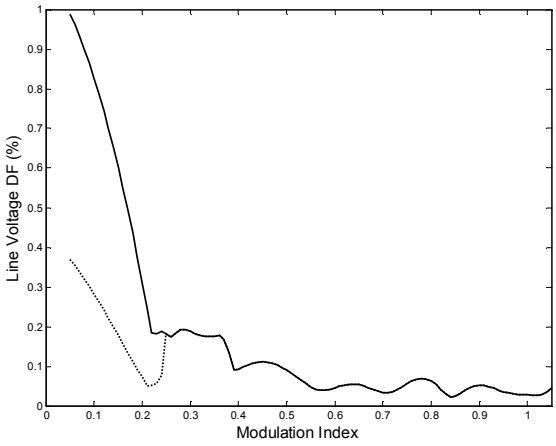


Fig. 10.
DF of line voltage versus modulation index, suggested (dotted curve) and ordinary (solid curve) techniques.

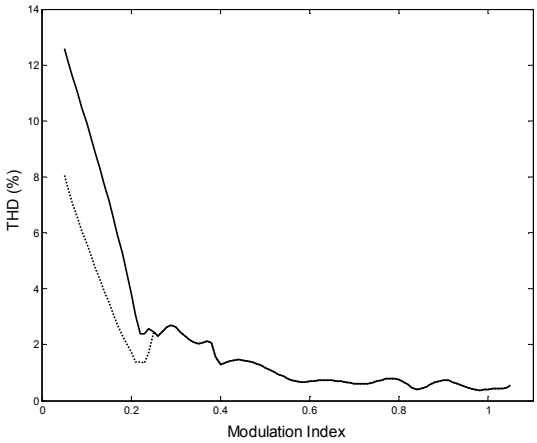


Fig. 11.
THD of line current versus modulation index, suggested (dotted curve) and ordinary (solid curve) techniques.

APPENDIX

Equations of Different Modulation Index Levels for Seven-Level Inverter

High level case:

$$\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)=\frac{3m\pi}{4}$$
$$\cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)=0$$
$$\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)=0$$

Middle level case:

$$\cos(\alpha_1)+\cos(\alpha_2)-\cos(\alpha_3)=\frac{3m\pi}{4}$$
$$\cos(5\alpha_1)+\cos(5\alpha_2)-\cos(5\alpha_3)=0$$
$$\cos(7\alpha_1)+\cos(7\alpha_2)-\cos(7\alpha_3)=0$$

Low level case:

$$\cos(\alpha_1)-\cos(\alpha_2)+\cos(\alpha_3)=\frac{3m\pi}{4}$$
$$\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)=0$$
$$\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)=0$$

Very low level case:

$$[\cos(\alpha_1)-\cos(\alpha_2)+\cos(\alpha_3)-\cos(\alpha_4)+\cos(\alpha_5)-\cos(\alpha_6)]=\frac{3m\pi}{4}$$

$$[\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)+\cos(5\alpha_5)-\cos(5\alpha_6)]=0$$

$$[\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)+\cos(7\alpha_5)-\cos(7\alpha_6)]=0$$

$$[\cos(11\alpha_1)-\cos(11\alpha_2)+\cos(11\alpha_3)-\cos(11\alpha_4)+\cos(11\alpha_5)-\cos(11\alpha_6)]=0$$

$$[\cos(13\alpha_1)-\cos(13\alpha_2)+\cos(13\alpha_3)-\cos(13\alpha_4)+\cos(13\alpha_5)-\cos(13\alpha_6)]=0$$

$$[\cos(17\alpha_1)-\cos(17\alpha_2)+\cos(17\alpha_3)-\cos(17\alpha_4)+\cos(17\alpha_5)-\cos(17\alpha_6)]=0$$