Control of DC link ripple eliminator with reduced capacitance for grid-connected power converters

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Abstract. Controller design for a ripple eliminator aimed to reduce the bulk capacitance of grid-connected converters and suppress the DC link ripple is revealed in the paper. The ripple eliminator is based on a small auxiliary capacitance, interfaced to the DC link by a bidirectional converter. The primary goal of the proposed system is regulating the DC link voltage, releasing the grid-interfacing converter from the task thus making possible to increase DC link voltage control bandwidth without sacrificing input power factor. The proposed system may be perceived as an output-voltage regulated wide-input-range boost converter feeding a bi-directional power load. The paper focuses on control analysis as well as on operational issues of the proposed ripple eliminator. The revealed findings are fully supported by simulations.

Key words

AC/DC power converters, DC link ripple, voltage regulation, stability.

1. Introduction

Instantaneous input power of practical power converters, connected to single-phase or unbalanced three-phase grids contains both DC and pulsating components. The DC part of grid power is transferred to the load and pulsating component is absorbed by an instantaneous power-matching element (typically a bulk DC link capacitor) [1]. In case the load is connected to the DC bus via power electronics interface, it may contribute pulsating power, which needs to be captured by the same power-matching element. Pulsating power absorbed by the bulk capacitance translates into DC-link voltage ripple, which must reside within predetermined limits, set restricted by grid-connected converter topology and the DC link capacitor voltage rating. This leads to necessity of utilizing electrolytic capacitors in applications of 50W and higher [2]. Consequently, reliability and physical size drawbacks related to electrolytic capacitors are brought into modern power electronics based energy conversion systems [3]. In order to tackle these shortcomings, two main groups of solutions were suggested in the literature, namely passive and active. The former is based on adding inductors to the DC link in order to realize a resonant filter, tuned to (typically low) fundamental frequency of the pulsating power [4]. In addition, more than single fundamental component may exist. Hence, massive DC link resonant filter banks are required. Active solutions do not require addition of bulky passive components and has therefore attracted much attention, focusing on three main research directions as follows.

- Since the power factor acceptable by different standards is typically lower than unity, it is possible to reduce the DC link capacitance by distorting the input current of the grid-interfacing converter [5]. Unfortunately, the achieved capacitance reduction ratio is relatively low due to tight grid code requirements, limiting the accepted distortion amount. Moreover, since grid codes are not universal, the proposed solution must be individually adopted for each case.

- Novel topologies, specially aimed to reduce the total DC link capacitor required, were proposed in [6], [7]. The main disadvantage of these converters is relatively nontrivial operation, requiring a from-scratch design in most of the cases. Moreover, most of the concepts presented are non-applicable to existing basic topologies.

- Replacing the bulk DC link capacitor by an additional power converter terminated by a much smaller capacitance is the main idea behind the most popular active capacitance reduction research direction [8] – [10]. The operation is based on the fact that the amount of DC link capacitor energy used comprises only small fraction of the stored energy, i.e. much lower capacitance is sufficient to absorb the pulsating power component once the capacitor voltage ripple constraints are released. Consequently, decoupling the DC link and the power matching capacitance by a bidirectional power converter allows significant reduction of capacitor value.

The paper focuses on the latter subgroup of solutions. The approach to DC link ripple mitigation by direct voltage regulation proposed in [11] is utilized. There, the pulsating current component is indirectly forced to be absorbed by the ripple eliminator, requiring DC link voltage sensing only. However, once the DC link voltage is directly

regulated by the ripple eliminator, it no longer reflects the power balance of the system, i.e. the voltage loop of the grid interfacing converter can no longer utilize the DC link voltage as system power balance indicator. Hence, auxiliary capacitor voltage is fed to the grid-interfacing converter voltage controller. The proposed system therefore allows "breaking" the tradeoff between the power factor and DC link voltage loop bandwidth, since the voltage loop of the grid interfacing converter is not related to the average value of the DC link voltage. Consequently, the DC link voltage quality becomes a function of the ripple eliminator regulation capabilities only.

This work reveals modeling and control design of the proposed system in detail. The proposed ripple eliminator is perceived as an output-voltage regulated wide-input-range boost converter feeding a bi-directional power load. Thus, control design is non-trivial and was neither mentioned nor analyzed in the literature by far. Moreover, modifying the feedback signal to an existing grid interfacing converter voltage controller is challenging too since the voltage ripple magnitude as well as the capacitance value of the ripple eliminator capacitor are different from the ones used to design the controller above.

2. The Proposed Ripple Eliminator

Consider an off-the shelf feedback controlled PFC front end, shown in Fig. 1(a) (the idea of using it is demonstrating that the proposed ripple eliminator may be combined with an existing GIC in a nearly plug-and-play fashion). The PFC front end consists of power stage and feedback controller, operating in a dual-loop arrangement while sensing DC link voltage and inductor (or switch) current, as shown. Bulk DC link capacitance is also present to absorb pulsating power component. The ripple eliminator (RE) replaces the bulk DC link capacitance as shown in Fig. 1(b), realized by a bidirectional converter terminated by reduced auxiliary capacitance. Small ceramic capacitor is connected across DC link-side terminals of the ripple eliminator to absorb the switching ripple. The auxiliary capacitance voltage and current are sensed as shown. The combined PFC+RE system is shown in Fig. 1(c). DC link voltage, auxiliary capacitance voltage and current measurements are fed to the ripple eliminator controller, which in turn drives the RE switches and creates feedback signal to the off-the-shelf PFC controller. Bulk DC link capacitance and original PFC voltage feedback branch are disconnected. The proposed control structure allows modifying the voltage feedback to the PFC controller only in order to implement the above mentioned PFC voltage loop variable change while leaving the rest of the PFC system unaltered. Small ceramic capacitor remains connected across DC link-side terminals of the PFC to absorb the switching ripple. To conclude, bulk capacitor disconnection and voltage feedback branch replacement are the only required modifications of the GIC. This is referred as "nearly plug-and-play" operation.
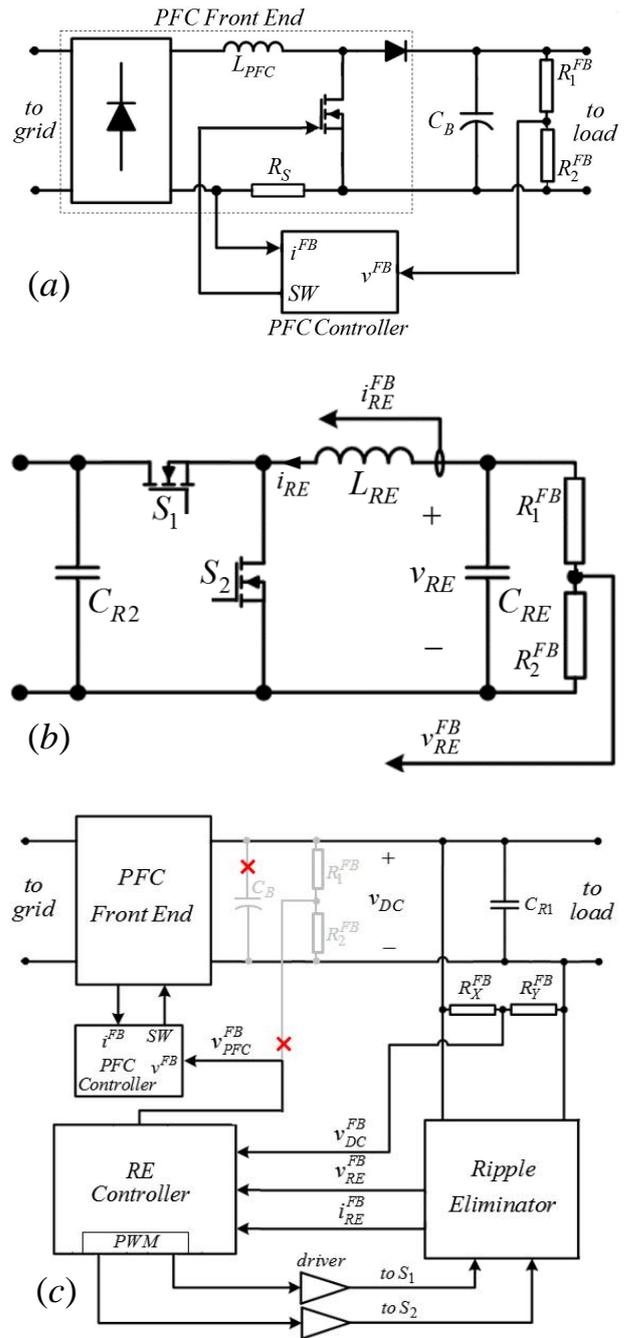
Fig. 1. The proposed system components: (a) off-the-shelf PFC front end; (b) the proposed ripple eliminator; (c) combined PFC+RE system.

3. Control Design

The control structure of the proposed ripple eliminator controller is shown in Fig. 2. Dual-loop voltage-current structure with (optional) voltage loop gain scheduling (GS) and current loop feed-forwarding (FF) is used to control the REC. The auxiliary capacitor voltage feedback is notch-filtered to remove the double-grid-frequency pulsating component and then shifted and scaled to create voltage feedback to the PFC controller.

Fig. 2. The proposed ripple eliminator controller structure.

The output of the current controller C_I satisfies

$$-1 < v_C(t) < 1. \tag{1}$$

Then, RE switching-cycle-averaged model with v_C as the control input is shown in Fig. 3.

Fig. 3. Switching-cycle-averaged model of the RE.

It may be concluded that the RE drives a bidirectional load while subject to widely varying input voltage. The RE large-signal dynamics is then governed by

$$C_{RE} \frac{dv_{RE}}{dt} = -i_{RE}$$

$$L_{RE} \frac{di_{RE}}{dt} = v_{RE} - \frac{1-v_C}{2} v_{DC} \tag{2}$$

$$C_R \frac{dv_{DC}}{dt} = \frac{1-v_C}{2} i_{RE} - \frac{p_3}{v_{DC}}$$

with $C_R = C_{R1} + C_{R2}$. The control-to-output transfer function is then obtained as

$$\frac{\tilde{v}_{DC}}{\tilde{v}_C}(s) =$$

$$\frac{V_{DC}^2}{2V_{RE}} \frac{L_{RE}C_{RE}s^2 - \frac{C_{RE}V_{RE}^2}{P}s + 1}{-\frac{V_{DC}^2 C_R L_{RE} C_{RE}}{P}s^3 + L_{RE}C_{RE}s^2 - \frac{C_R V_{DC}^2 + C_{RE}V_{RE}^2}{P}s + 1}, \tag{3}$$

linearized around the (time-varying) operating point, given by (in steady-state)

$$P(t) = -P_1 \cos 2(\omega_1 t + \theta_1),$$

$$V_{RE}(t) = V_{RE}^* \sqrt{1 - \frac{P_1}{\omega_1 (V_{RE}^*)^2 C_{RE}} \sin 2(\omega_1 t + \theta_1)}. \tag{4}$$

According to (4), $P(t)$ possesses periodically alternating polarity. As long as P is negative (i.e. the ripple eliminator supplies power to the DC link), the control-to-output transfer function is stable, containing two stable zeros, and may be stabilized utilizing any of known classical methods. However, when the ripple eliminator absorbs power from the DC link (i.e. P is positive), (3) becomes unstable in addition to containing two unstable zeros. In this case, stabilization is nontrivial and challenging. Moreover, it is extremely difficult to design a unified controller, suitable for both cases. A dual-loop configuration is adopted here as the starting design point. Consider the classical approach of current loop shaping, i.e. v_{RE} and v_{DC} are assumed independent, slow-varying disturbances from the current loop point of view. Then, the small-signal version of current-loop-related part (2) is given by

$$\tilde{i}_{RE} = \frac{V_{DC}}{2L_{RE}s}(\tilde{v}_C + \tilde{v}_D) \tag{5}$$

with

$$\tilde{v}_D = \frac{2}{V_{DC}}\left(\tilde{v}_{RE} - \frac{V_{RE}}{V_{DC}}\tilde{v}_{DC}\right) \tag{6}$$

denoting the total current loop disturbance. Simplified control-to-ripple eliminator current transfer function is

$$P_{CI}(s) = \frac{\tilde{i}_{RE}(s)}{\tilde{v}_C(s)} = \frac{\frac{V_{DC}}{2}}{L_{RE}s}. \tag{7}$$

Selecting a PI controller

$$C_I(s) = \frac{K_{PI}s + K_{II}}{s} \tag{8}$$

as current loop regulator, there is

$$\tilde{i}_{RE}(s)\big|_{\tilde{v}_D(s)=0} = T_I(s)i_{RE}^*(s) \tag{9}$$

with

$$T_I(s) = \frac{\frac{V_{DC}}{2L_{RE}}K_{PI}s + \frac{V_{DC}}{2L_{RE}}K_{II}}{s^2 + \frac{V_{DC}K_{PI}}{2L_{RE}}s + \frac{V_{DC}K_{II}}{2L_{RE}}} \tag{10}$$

i.e. unity tracking DC gain and zero disturbance rejection DC gain are assured. Nevertheless, note that in this case ripple eliminator voltage and ripple eliminator current are coupled as

$$\tilde{v}_{RE} = -\frac{1}{C_{IN}s}\tilde{i}_{RE}. \tag{11}$$

Hence, (5) turns into is

$$\tilde{i}_{RE} = \frac{C_{RE}s}{L_{RE}C_{RE}s^2 + 1}\frac{V_{DC}}{2}(\tilde{v}_C + \tilde{v}_D) \tag{12}$$

with

$$\tilde{v}_D = -\frac{2V_{RE}}{V_{DC}^2}\tilde{v}_{DC}. \tag{13}$$

Full control-to-ripple eliminator current transfer function is then

$$P_{CI}(s) = \frac{\frac{V_{DC}}{2}C_{RE}s}{L_{RE}C_{RE}s^2 + 1}. \tag{14}$$

possessing two undamped poles (in reality these are lightly damped poles due to parasitic resistances). Consequently, utilizing (8) as loop controller yields (9) with

$$T_I(s) = \frac{\frac{V_{DC}K_{PI}}{2L_{RE}}s + \frac{V_{DC}K_{II}}{2L_{RE}}}{s^2 + \frac{V_{DC}K_{PI}}{2L_{RE}}s + \frac{1}{L_{RE}C_{RE}} + \frac{V_{DC}K_{II}}{2L_{RE}}} \tag{15}$$

i.e. zero disturbance rejection DC gain is assured. The tracking low-frequency gain is non-unity, given by

$$T_I(s \to 0) = \cfrac{1}{1 + \cfrac{2}{C_{RE}V_{DC}K_{II}}}, \qquad (16)$$

i.e. some steady-state current tracking error is expected, which can be minimized (but not eliminated) by increasing C_{RE}, V_{DC} and/or K_{II}.

It is possible to completely eliminate the steady-state current tracking error as shown in Fig. 2 by adding a feedforward term

$$v_{FF} = 1 - \frac{2v_{RE}}{v_{DC}} \qquad (17)$$

to the control signal v_C, turning the second equation of (2) into

$$L_{RE}\frac{di_{RE}}{dt} = \frac{1}{2}v_C v_{DC} \qquad (18)$$

thus "breaking" the current loop dependence on v_{RE}. Linearizing, there is

$$\tilde{i}_{RE} = \frac{V_{DC}}{2L_{RE}s}\left(\tilde{v}_C + \tilde{v}_D\right) \qquad (19)$$

with

$$\tilde{v}_D = \frac{V_{DC} - 2V_{RE}}{V_{DC}^2}\tilde{v}_{DC}. \qquad (20)$$

Utilizing (17) retains (10), bringing back both unity tracking DC gain and zero disturbance rejection DC gain. Moreover, once DC link voltage is tightly regulated, its constant reference value V_{DC}^* may be used in (17) instead of measured v_{DC}.

When current and voltage loops are decoupled in frequency domain and the former is well-designed, $i_{RE} = T_I(0)i_{RE}^*$ may be assumed. Assuming $T_I(0) = 1$, DC link voltage small-signal dynamics is obtained as

$$\tilde{v}_{DC}\big|_{\tilde{p}=0} = P_{CV}(s)\tilde{i}_{RE}^* \qquad (21)$$

with

$$P_{CV}(s) = \frac{-P}{C_R V_{DC}C_{RE}V_{RE}} \frac{L_{RE}C_{RE}s^2 - \dfrac{V_{RE}^2 C_{RE}}{P}s + 1}{s^2}. \qquad (22)$$

The inductor-induced zero resides significantly outside the control bandwidth for all possible operation points; therefore, the control-to-output transfer function may be simplified as

$$P_{CV}(s) \approx G\frac{1 + \omega_Z^{-1}s}{s^2} \qquad (23)$$

with

$$G = \frac{-P}{C_R V_{DC}V_{RE}C_{RE}}, \quad \omega_Z^{-1} = -\frac{V_{RE}^2}{P}C_{RE}. \qquad (24)$$

When the pulsating power reverses its direction, both gain and zero reverse polarities as well. In general, in case the control-to-output transfer function reverses polarity, the controller sign must be inverted as well to preserve stability. Moreover, different controllers should be designed for each pulsating power polarity to have similar closed loop dynamics in both cases. Here, we propose a non-traditional yet simple approach allowing to utilize the

same controller for both cases as follows. First, consider the operating point in which $P = 0$. Then,

$$P_{CV}(s) = \frac{V_{RE}}{C_R V_{DC}s} \qquad (25)$$

and utilizing a PI controller

$$C_V = \frac{K_{PV}s + K_{IV}}{s} \qquad (26)$$

brings the system to

$$\tilde{v}_{DC}(s)\big|_{\tilde{p}(s)=0} = T_V(s)i_{RE}^*(s) \qquad (27)$$

with

$$T_V(s) = \cfrac{\dfrac{V_{RE}K_{PV}}{C_R V_{DC}}s + \dfrac{V_{RE}K_{IV}}{C_R V_{DC}}}{s^2 + \dfrac{V_{RE}K_{PV}}{C_R V_{DC}}s + \dfrac{V_{RE}K_{IV}}{C_R V_{DC}}} \qquad (28)$$

i.e. unity tracking DC gain and zero disturbance rejection DC gain are assured. Using (26) with the general control-to-output transfer function (28) yields

$$T_V(s) = \frac{GK_{PV}\omega_Z^{-1}s^2 + G\left(K_{PV} + K_{IV}\omega_Z^{-1}\right)s + GK_{IV}}{s^3 + GK_{PV}\omega_Z^{-1}s^2 + G\left(K_{PV} + K_{IV}\omega_Z^{-1}\right)s + GK_{IV}}. \qquad (29)$$

At the first glance, (29) appears to possess unity DC gain, as desired. Nevertheless, G and ω_Z^{-1} are negative when $P > 0$ and since the coefficients of PI controller (26) are positive, (29) contains an unstable pole and hence its step response diverges. On the other hand, when $P < 0$, no instability occurs and step response of (29) is expected to converge. Furthermore, (29) may be decomposed into partial fractions as

$$T_V(s) = \frac{k_1}{s + \omega_{P1}} + \frac{k_1^*}{s + \omega_{P1}^*} + \frac{k_3}{s + \omega_{P3}}. \qquad (30)$$

In case the partial fraction gain of the unstable mode is significantly lower that these of the stable modes, the short-time behavior would dominated by the stable poles pair and not diverge during the unstable half cycle.

It is possible to further improve the dynamics of the voltage loop by gain scheduling as follows. According to (25), the gain of the control-to-output voltage loop transfer function is proportional to v_{RE}, which is time-varying. Since the voltage across the RE auxiliary capacitance is measured, it may be used in a gain-scheduling fashion to eliminate the dependence on v_{RE}, as shown in Fig. 2.

As stated in the preceding Section, when utilizing the proposed ripple eliminator, system power balance is reflected by RE auxiliary capacitance rather than DC link voltage. Since PFC voltage controller task is maintaining system power balance, it should now rely on v_{RE} rather than v_{DC}. However, two problems arise. First, design of the PFC controller voltage loop compensator is based on the value of bulk DC link capacitance C_B rather than on C_{RE}. Utilizing the controller gain designed according to C_B for operation with $C_{RE} << C_B$ would increase the bandwidth of PFC voltage loop and as a result PFC input current would be distorted. The following may be performed to solve the issue. As shown in [1], PFC voltage loop bandwidth is proportional to the DC value of the loop gain $L(0)$ and inversely proportional to the bulk capacitance value,

$$\omega_{V,PFC} \sim \frac{L(0)}{C_B}. \qquad (31)$$

Moreover, the original loop bandwidth (typically set to around one-fifth of the fundamental grid frequency) should not be altered to maintain input current quality and original PFC dynamics. Consequently, in case C_{RE} is used instead of C_B, the loop gain must be modified accordingly to preserve $\omega_{V,PFC}$. This may be accomplished either by altering either the feedback compensator gain or the feedback path slope. The latter is preferable since it allows keeping the original PFC controller as is while the feedback path can easily be modified by the RE controller.

Second, auxiliary capacitance voltage ripple is much higher than the original DC link. Consequently, undervoltage/overvoltage detection limits may be violated when feedig back high-ripple signal to the PFC controller. This will trip the undervoltage/overvoltage protection, preventing normal operation. In order to eliminate the problem of excessive ripple, auxiliary capacitance voltage may e.g. be notch-filtered at double-grid-frequency to eliminate the dominant harmonic.

4. Validation by simulation

Simulation results are obtained using data given in Table I. PI controller design should maximize current loop bandwidth for the desired phase margin φ_M while taking into account switching delay T_d. Here, $\varphi_M = 45^o$ was selected and $T_d = T_S$ was assumed, leading to crossover frequency of ~4kHz. Simulation results shown in Fig. 4 demonstrate current loop performance without and with feedforward action for rated load operation (actual inductor current is notch-filtered to remove the switching ripple harmonic for clarity). Nonzero steady state error is noticeable in the former case while in the latter case it is eliminated, as expected.

TABLE I.
SYSTEM PARAMETER VALUES

Parameter	Value	Units
Switching frequency, T_S^{-1}	50	kHz
REC inductance, L_{RE}	320	μH
REC capacitance, C_{RE}	22	μF
Total DC link capacitance, C_R	9.4	μF
Grid frequency, ω_1	100π	rad/s
Reference voltage, V_{RE}^*	271	V
Reference voltage, V_{DC}^*	400	V
Rated load power, $P_{2,MAX}$	360	W

The crossover frequency of the voltage loop was selected as 800Hz (one-fifth of the current loop bandwidth) to allow decent loop decoupling. Apparently, the real part of ω_{P3} is positive for $P > 0$, as expected. Despite this, the partial fraction gain of the unstable mode is significantly lower (three orders of magnitude) that these of the stable modes. This indicates that the short-time behavior is dominated by the stable poles pair.

Since in 50Hz grid $P > 0$ for 5ms, in case stable poles dominance lasts more than that, the system is referred to as *short-time stable* and the unstable pole would not be sufficient to influence the stability in such short interval.
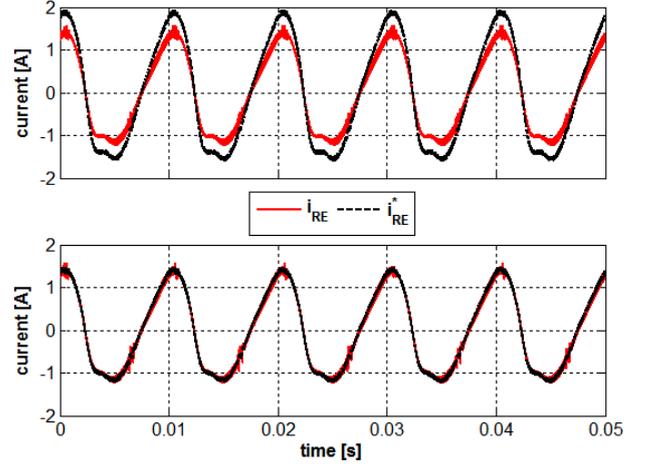

Fig. 4. Simulation results: ripple eliminator reference and actual currents without (top) and with (bottom) feedforward action (rated load operation).

Simulation results shown in the top subplot of Fig. 5 compare voltage loop performance (rated load operation) of the four following cases: with 270μF electrolytic capacitor (the curve labeled "EC"); with dual-loop controlled ripple eliminator (without feedforward and gain scheduling actions, the curve labeled "basic RE"), with dual-loop controlled ripple eliminator (with feedforward action but without gain scheduling, the curve labeled "RE with FF") and with dual-loop controlled ripple eliminator (with both feedforward and gain scheduling actions, the curve labeled "RE with FF and GS"). Apparently, the ripple eliminator based system is expected to outperform electrolytic capacitor based system in terms of pear-to-peak ripple magnitude (yet possessing higher harmonic content). Moreover, adding feedforward and gain scheduling actions further improves the DC link voltage quality (without significantly affecting the REC auxiliary capacitance voltage, as shown in the bottom subplot of Fig. 6). In addition, it may be concluded that marginal improvement of adding current loop feedforward action is much more noticeable than that of voltage loop gain scheduling addition.
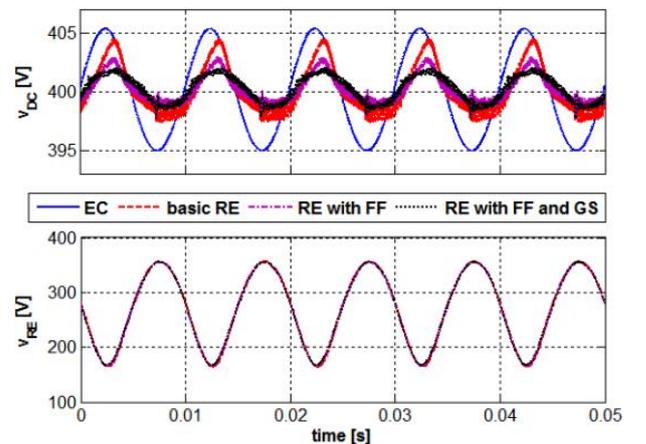

Fig. 5. Simulation results: DC link (top) and ripple eliminator auxiliary capacitance (bottom) voltages.

Auxiliary capacitance voltage ripple is much higher than the original DC link ripple (~200V versus ~12V). Internal

reference voltage of the off-the-shelf PFC controller is 5V, i.e. 1/80 voltage divider is employed to scale the 400V DC link voltage. The 12V DC link ripple is then scaled to 0.15V feedback signal ripple. Undervoltage/overvoltage detection limits are set to 4.75V and 5.25V, respectively. In case v_{RE} is scaled down from 271V down to 5V, its 200V ripple turns into 3.7V feedback signal ripple, as shown in the top subplot of Fig. 6. This will trip the undervoltage/overvoltage protection of the PFC controller, preventing normal operation. Therefore, the PFC feedback signal is synthesized according to the following relation,

$$v_{PFC}^{FB} = 5 + \frac{1}{80\frac{C_B}{C_{RE}}}\left(NF\{v_{RE}\} - V_{RE}^*\right) \qquad (32)$$

with α_C defined in (23). Apparently, in case the filtered value of v_{RE} equals 271V, 5V level is fed back to the PFC controller, as required. Otherwise, the difference is scaled down by $80 \cdot C_B/C_{RE}$ to account for both 400V-to-5V conversion gain expected by the PFC controller and loop gain manipulation. The bottom subplot of Fig. 7 demonstrates the synthesized feedback voltage to the PFC controller. Note that the ripple is well within the permitted range. Moreover, it is well evident that after passing through a 100Hz notch filter, the ripple is dominated by 200Hz harmonic, as predicted in the preceding paragraph discussion).
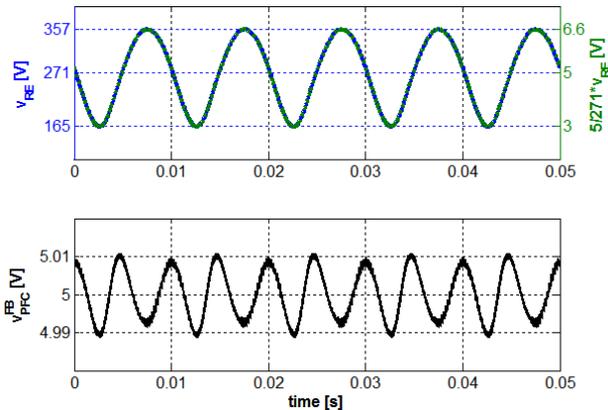

Fig. 6. Simulation results: Top - actual and scaled REC auxiliary capacitance voltage; Bottom – synthesized PFC controller feedback voltage.

4. Conclusion

Control design of the novel DC link ripple eliminator with reduced capacitance for grid interfacing converters were revealed in the paper. The proposed approach allowed increasing the bandwidth of DC link voltage control loop without sacrificing input power factor. On the other hand, the auxiliary capacitance of the proposed ripple eliminator was shown to reflect the power balanced of the system and hence the grid-interfacing converter voltage controller regulates its average value, taking into account the underlying operational restrictions. The proposed ripple eliminator was shown to resemble an output-voltage regulated wide-input-range boost converter feeding a bi-directional power load. Dual-loop control structure with current feedforward and voltage gain scheduling was

formed to cope with the control challenge. Simulation results of applying the proposed control method to an off-the-shelf PFC front end support the proposed control system.

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